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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,306	04/24/2001	Bunji Mizuno	60188-063	4390

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WASHINGTON, DC 20005-3096

EXAMINER
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SARKAR, ASOK K

ART UNIT	PAPER NUMBER
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2829

DATE MAILED: 03/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/840,306	MIZUNO ET AL.
	Examiner Asok K. Sarkar	Art Unit 2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 24 April 2001.
- 2a) This action is FINAL.                  2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-38 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. 08/734,218.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a)  The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                 | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                        | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>H5</u> | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### ***Information Disclosure Statement***

1. Three foreign documents (China, Korea and Taiwan) in the information disclosure statement filed April 24, 2001 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

### ***Specification***

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Method of manufacturing semiconductor device by sputter-doping".

Under section "Related Application", please insert -- now US 6,217,951, -- after filed October 21, 1996.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 5, 6, 20, 22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booske, US 5,672,541 in view of Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2, Chapter 2, Lattice Press, 1990.

Regarding claims 1, 5, 20 and 24, Booske teaches a fabrication method for semiconductor devices such as diode and transistor (column 7, lines 57 – 67) by the process of plasma source ion implantation (PSII) comprising the steps of:

- holding the semiconductor substrate 20 in the vacuum chamber (see Fig. 1) in column 8, lines 31 – 35 and the impurity solid including impurity (46 and 52) to be introduced into the diode or the transistor formation region in the vacuum chamber (see Fig. 1) in column 4, lines 27 - 33;
- introducing an inert/noble gas in column 8, lines 28 – 29 to generate the plasma;
- applying a first voltage to the impurity solid target to serve as a cathode for the plasma, performing sputtering and thereby mixing the impurity from the solid target into the plasma in various places of the disclosure such as in column 7, lines 1 - 2
- applying a second voltage to the semiconductor substrate to serve as cathode in column 11, line 28 so that the impurity mixed with the plasma is introduced directly to the surface portion of the device formation region to form an impurity layer (region 34 in Fig. 3), and
- forming an inter connection layer to electrically connect the impurity layer in column 13, lines 45 – 57) as shown in Fig. 6.

Booske fails to expressly teach electrically isolating the diode or the transistor formation region on the substrate by an element isolation layer.

Wolf discloses in Chapter 2 that device isolation is necessary when fabricating ICs so that the devices can subsequently be interconnected to create desired circuit configurations.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify the method of Booske by adding an electrically isolating the diode or the transistor formation region on the substrate by some form of an element isolation layer as taught by Wolf so that the devices can subsequently be interconnected to create desired circuit configurations.

Regarding claims 3 and 22, Booske teaches impurity layers containing components from the reactive impurity gas in column 3, lines 6 – 14.

Regarding claims 6 and 25, Booske teaches silicon substrate in column 8, line 40, impurity of B and P in column 5, lines 27 – 34 and reactive gas including Ar in column 8, line 27.

5. Claims 2 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booske, US 5,672,541 in view of Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2, Chapter 2, Lattice Press, 1990 as applied to claims 1 and 20 above, and further in view of Nakagawa, JP 05024976 and Yamazaki, US 5,789,292.

Booske in view of Wolf fails to teach irradiation of a laser beam on the semiconductor substrate during plasma doping.

Nakagawa teaches a doping method, which includes irradiation of an ultraviolet

radiation on the semiconductor substrate (see the claims).

Booske in view of Wolf and further in view of Nakagawa fails to expressly teach irradiation of a laser beam on the semiconductor substrate.

Yamazaki teaches a method of laser doping in which laser beam is irradiated on the substrate on the semiconductor substrate (see abstract of the disclosure).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to form the device by irradiating a laser beam at an ultraviolet wave length on the semiconductor substrate as taught by Yamazaki instead of the ultraviolet light taught by Nakagawa since the doping process can be better controlled by controlling the laser radiation.

6. Claims 4 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booske, US 5,672,541 in view of Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2, Chapter 2, Lattice Press, 1990 as applied to claims 3 and 22 above, and further in view of Zhang, US 5,320,984.

Booske in view of Wolf fails to teach the concentration of the components of the inert gas exceeding  $1 \times 10^{20} \text{ cm}^{-3}$ .

Zhang teaches doping the target with impurity concentration higher than  $1 \times 10^{17}$  atoms. $\text{cm}^{-3}$  in column 3, lines 24 – 25.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to generate a concentration of the components of the inert gas of Booske's method exceeding  $1 \times 10^{20} \text{ cm}^{-3}$  as taught by Zhang since this level of concentration will be necessary for proper doping of the substrate.

7. Claims 7, 9, 11, 12, 13, 26, 28, 30, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booske, US 5,672,541 and Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2, Chapter 2, Lattice Press, 1990 in view of Nakagawa, JP 05024976.

Regarding claims 7 and 26, Booske and Wolf teach most of the limitations of These claims as has been explained above with respect to claims 1 and 20.

Booske and Wolf fail to expressly teach applying a second voltage to the semiconductor substrate to serve as anode so that the impurity mixed with the plasma is introduced directly to the surface portion of the device formation region to form an impurity layer.

Nakagawa teaches a method of semiconductor doping in which the first voltage to the impurity target serves as cathode (104 in Fig. 1) and the second voltage applied to the substrate serving as anode (103 in Fig. 1).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to form the device as taught by Booske by the use of an apparatus as taught by Nakagawa since doping regions of Booske's devices can be formed by using Nakagawa's apparatus.

Regarding claims 9 and 28, Booske teaches impurity layers containing components from the reactive impurity gas in column 3, lines 6 – 14.

Regarding claims 11, 12, 30 and 31, Booske teaches negative voltages for both the target and the substrate as was explained above in rejecting claims 1 and 20.

Regarding claims 13 and 32, Booske teaches silicon substrate in column 8, line 40, impurity of B and P in column 5, lines 27 – 34 and reactive gas including Ar in column 8, line 27.

8. Claims 8 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booske, US 5,672,541 and Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2, Chapter 2, Lattice Press, 1990 in view of Nakagawa, JP 05024976 as applied to claims 7 and 26 above, and further in view of Yamazaki, US 5,789,292.

Booske and Wolf in view of Nakagawa teaches a doping method, which includes irradiation of an ultraviolet radiation on the semiconductor substrate (see Nakagawa's claims).

Booske and Wolf in view of Nakagawa fails to expressly teach irradiation of a laser beam on the semiconductor substrate.

Yamazaki teaches a method of laser doping in which laser beam is irradiated on the substrate on the semiconductor substrate (see abstract of the disclosure).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to form the device by irradiating a laser beam at an ultraviolet wave length on the semiconductor substrate as taught by Yamazaki instead of the ultraviolet light taught by Nakagawa since the doping process can be better controlled by controlling the laser radiation.

Claims 10 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booske, US 5,672,541 in view of Nakagawa, JP 05024976 as applied to claims 9 and 28 above, and further in view of Zhang, US 5,320,984.

Booske in view of Nakagawa fails to teach the concentration of the components of the inert gas exceeding  $1 \times 10^{20} \text{ cm}^{-3}$ .

Zhang teaches doping the target with impurity concentration higher than  $1 \times 10^{17} \text{ atoms.cm}^{-3}$  in column 3, lines 24 – 25.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to generate a concentration of the components of the inert gas of Booske's method exceeding  $1 \times 10^{20} \text{ cm}^{-3}$  as taught by Zhang since this level of concentration will be necessary for proper doping of the substrate.

9. Claims 14, 16, 18, 19, 33, 35, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booske, US 5,672,541 and Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2, Chapter 2, Lattice Press, 1990 in view of Nakagawa, JP 05024976 and Stirn, US 4,596,645.

Regarding claims 14 and 33, Booske and Wolf in view of Nakagawa teaches most of the limitations of these claims as has been explained above with respect to claims 1, 7 20 and 26.

Booske in view of Nakagawa fails to expressly teach applying a first voltage to the impurity solid target material to allow the impurity solid target act as an anode.

Stirn teaches a sputtering process from an impurity target tin which the targets is biased to attract negatively ionized inert gas (see the abstract of the disclosure).

Stirn fails to expressly teach applying a positive potential to the target to serve it as an anode.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to form the device as taught by Booske by the use of an apparatus where the substrate is kept at a positive potential as taught by Nakagawa and the target is kept at a positive potential since negatively charged ions of the plasma will be attracted by the positively charged target for sputtering impurity ions from the target.

Regarding claims 16 and 35, Booske teaches impurity layers containing components from the reactive impurity gas in column 3, lines 6 – 14.

Regarding claims 18 and 37, Booske teaches negative voltages for both the target and the substrate as was explained above in rejecting claims 1 and 20.

Regarding claims 19 and 38, Booske teaches silicon substrate in column 8, line 40, impurity of B and P in column 5, lines 27 – 34 and reactive gas including Ar in column 8, line 27.

10. Claims 15 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booske, US 5,672,541 and Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2, Chapter 2, Lattice Press, 1990 in view of Nakagawa, JP 05024976 and Stirn, US 4,596,645 as applied to claims 14 and 33 above, and further in view of Yamazaki, US 5,789,292.

Booske and Wolf in view of Nakagawa and Stirn teaches a doping method, which includes irradiation of an ultraviolet radiation on the semiconductor substrate (see Nakagawa's claims).

Booske and Wolf in view of Nakagawa and Stirn fails to expressly teach irradiation of a laser beam on the semiconductor substrate.

Yamazaki teaches a method of laser doping in which laser beam is irradiated on the substrate on the semiconductor substrate (see abstract of the disclosure).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to form the device by irradiating a laser beam at an ultraviolet wave length on the semiconductor substrate as taught by Yamazaki instead of the ultraviolet light taught by Nakagawa since the doping process can be better controlled by controlling the laser radiation.

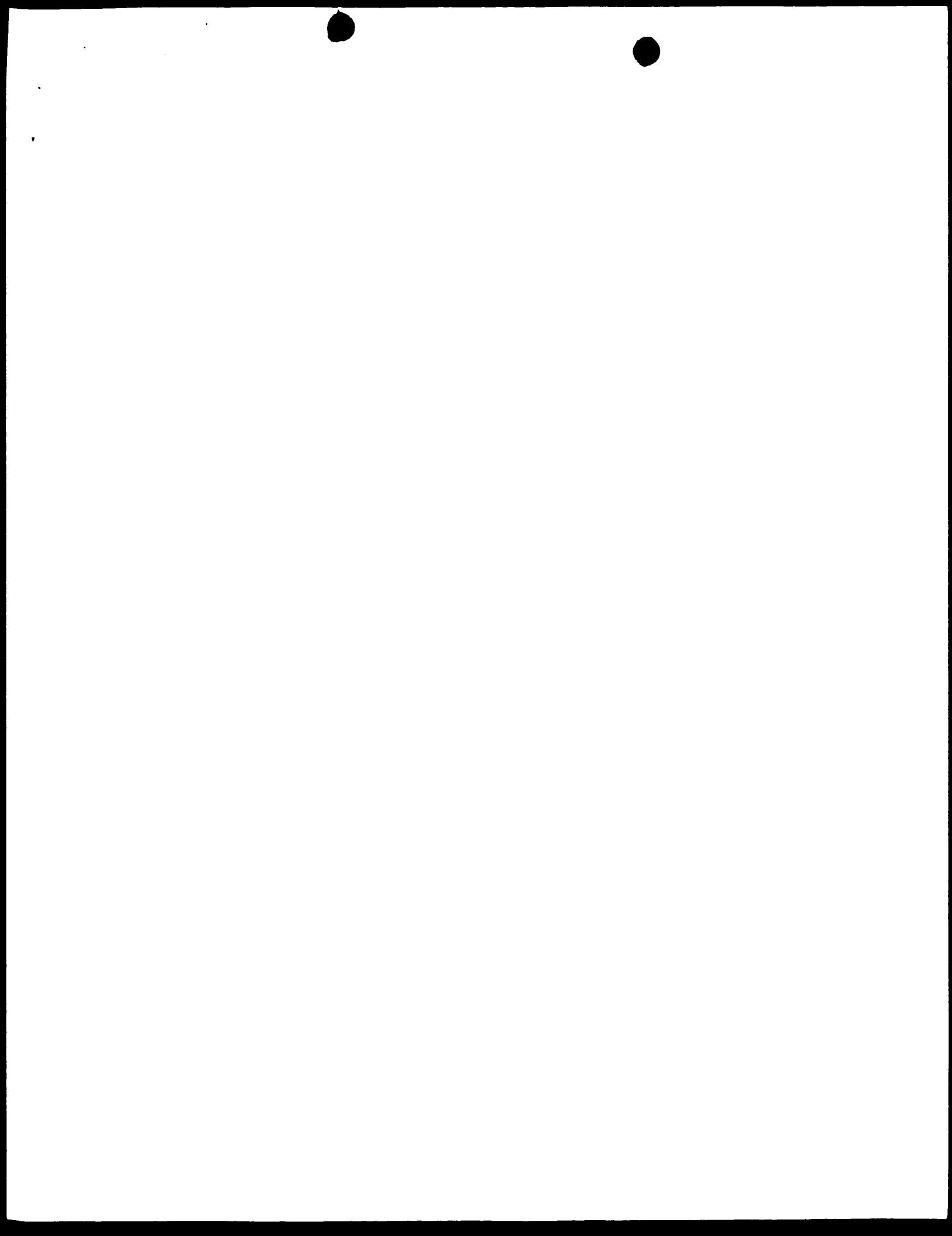
11. Claims 17 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booske, US 5,672,541 and Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2, Chapter 2, Lattice Press, 1990 in view of Nakagawa, JP 05024976 and Stirn, US 4,596,645 as applied to claims 16 and 35 above, and further in view of Zhang, US 5,320,984.

Booske and Wolf in view of Nakagawa and Stirn fails to teach the concentration of the components of the inert gas exceeding  $1 \times 10^{20} \text{ cm}^{-3}$ .

Zhang teaches doping the target with impurity concentration higher than  $1 \times 10^{17}$  atoms. $\text{cm}^{-3}$  in column 3, lines 24 – 25.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to generate a concentration of the components of the inert gas of Booske's method exceeding  $1 \times 10^{20} \text{ cm}^{-3}$  as taught by Zhang since this level of concentration will be necessary for proper doping of the substrate.

### ***Conclusion***



Art Unit: 2829

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 703 238 2521. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Sherry can be reached on 703 308 1680. The fax phone numbers for the organization where this application or proceeding is assigned are 703 308 7722 for regular communications and 703 308 7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 4918.

Asok K. Sarkar  
March 21, 2002



Michael J. Sherry  
3-21-02